

**lab report 9**

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In experiment 1)  
we are trying to build a cache system, so we modified on the data memory we created before

**module** DataMem (**input** clk, **input** MemRead, **input** MemWrite, **input** [**9**:**0**] addr // larger in size because it contains the word offset and the index

, **input** [**31**:**0**] data\_in, **output** **reg** [**127**:**0**] MsDataOut,//32\*4 cause the mem sends a whole block that contains 4 words

**output** **reg** Msready // represents that the mem finished reading or writing);

**reg** [**31**:**0**] mem [**0**:**1023**];//1KB memory , larger mem size

**wire**[**9**:**0**] bAddr;

**assign** bAddr = {addr[**9**:**2**],**2'b00**}; // neglecting the first 2 bits cause we don’t need the word offset, we need the block index

**always** @(posedgeclk)

Begin

Msready <= **0**; // initializing it with zero to be changed afterwards

**if** (MemWrite)

**begin**

**repeat** (**3**) **begin**// Wait for 3 clock cycles

@ (**posedge** clk);

End

mem[addr] <= data\_in;

Msready <= **1**; // mem finished writing

End

**else** **if** (MemRead)

Begin **repeat** (**3**) **begin**@ (**posedge** clk);

End

//reading a whole block,4 words

MsDataOut<={mem[bAddr],mem[bAddr+**1**],mem[bAddr+**2**],mem[bAddr+**3**]};

Msready <= **1**; // mem finished reading

End

End

**initial** **begin**

mem[**0**]=**32'd17**;

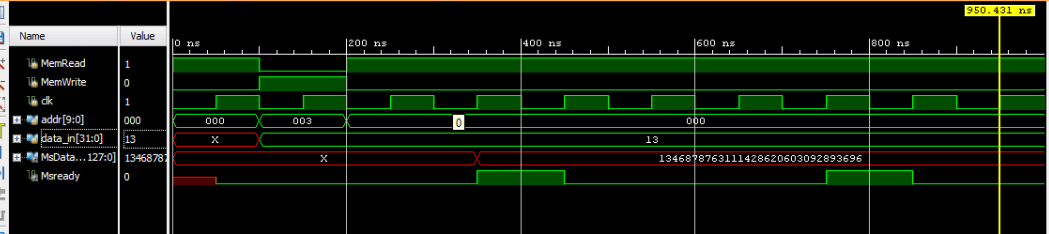
mem[**1**]=**32'd9**;

mem[**2**]=**32'd25**;

endendmodul

Test bench:

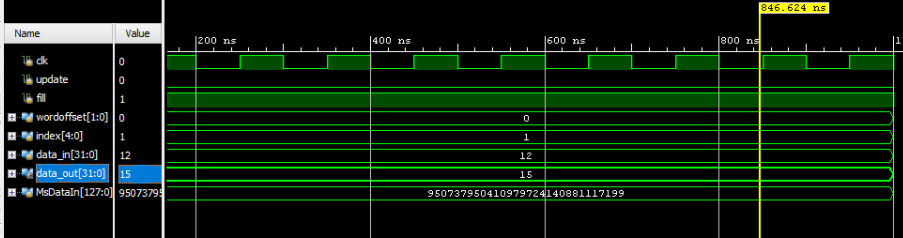
|  |
| --- |
| **`timescale** **1**ns / **1**ps      **module** datamem\_tb( );  **reg** MemRead;  **reg** MemWrite;  **reg** clk;  **reg**[**9**:**0**] addr;  **reg** [**31**:**0**] data\_in;  **wire** [**127**:**0**] MsDataOut;  **wire** Msready;    DataMem chace ( clk, MemRead, MemWrite, addr, data\_in, MsDataOut, Msready);  **initial**  **begin**  clk = **0**;  **forever** #**50** clk = ~clk;  **end**  **initial**  **begin**  // lw mn mem [0]    MemRead = **1** ;  MemWrite = **0** ;  addr = **0** ;    #**100**  // sw f mem[3] = 13    MemRead = **0** ;  MemWrite = **1** ;  addr = **3** ;  data\_in = **32'd13** ;  #**100**  MemRead = **1** ;  MemWrite = **0** ;  addr = **0** ;      **end**    **endmodule** |



Experiment 2:

Now we want to make a cache memory, which is of course smaller than the data memory

Here is the result of the simulation:



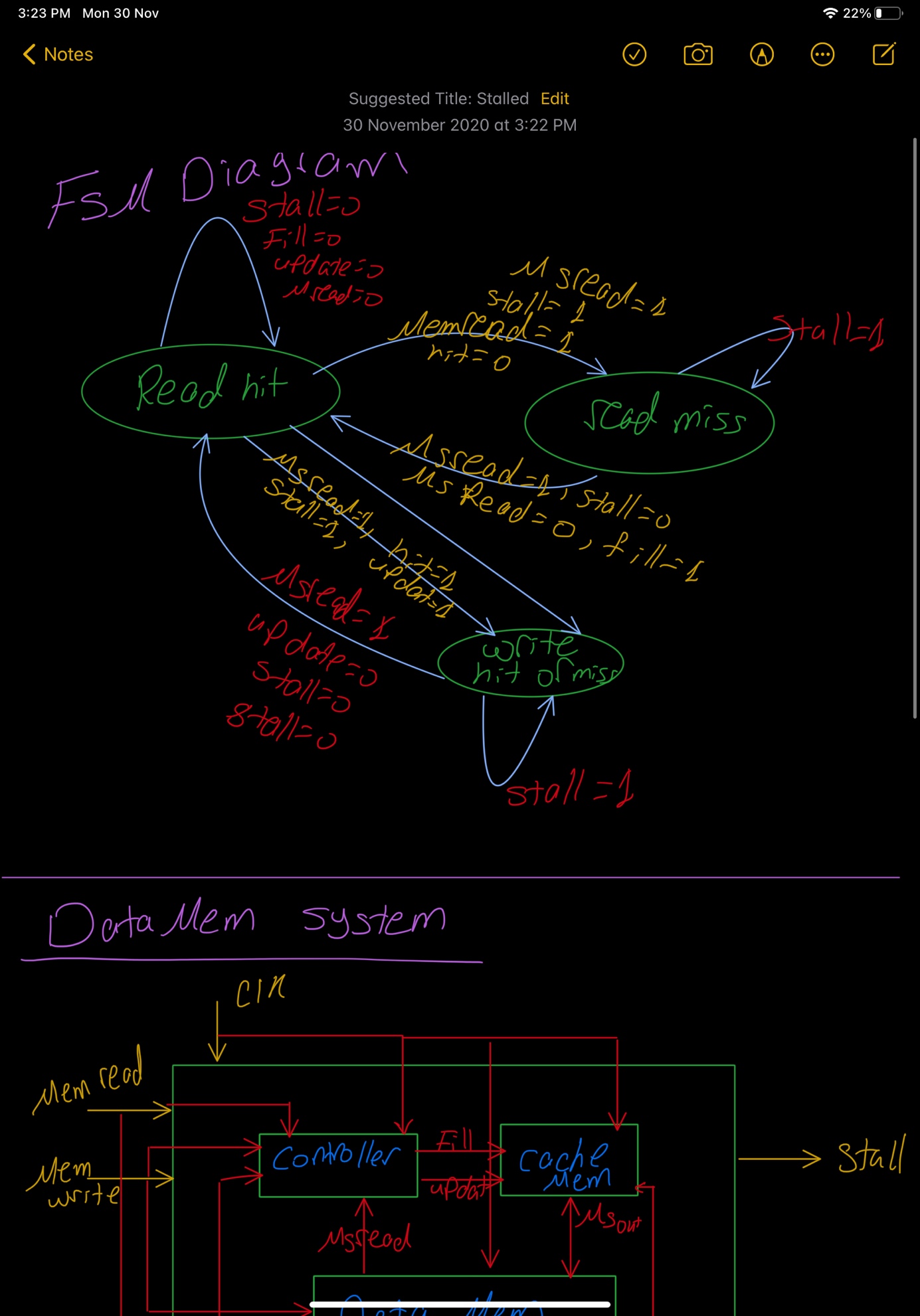
Difference:

Output was 32 bits

Now it is 128 bits

Also there is a delay 3 cycles to read 4 words ,   
it was reading just 1 word

FSM diagram



Data Mem system:

